Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (CURRENTLY AMENDED) A method of performing single bit error corrected M-bit words that have been scrambled using a self synchronizing scrambler, the method comprising the steps of:

a) calculating an N-bit CRC every K words of a block of J words using a generator polynomial, where J is a non-zero integer multiple of K;

b) forming an M-bit word from the calculated N-bit CRCs, where M is a non-zero integer multiple of N, and appending ~~this word~~ the said M-bit word to the block of J words to form a block of J+1 words for transmission;

c) calculating, responsive to receiving a block of J+1 words, another N-bit CRC every K words of the first J words of the received block of J+1 words and using, from the appended word, the N-bit CRC corresponding to the K words in each calculation; and

d) correcting, responsive to one of the another N-bit CRCs, computed at [[the]] a receiver, having a non-zero value, an errored bit in the received block of J+1 words, the errored bit being indicated by an entry in a table indexed according to the non-zero value.

2. (ORIGINAL) The method as defined in claim 1 wherein the M-bit words are 64b/66b encoded words (M=64 bits).

3. (ORIGINAL) The method as defined in claim 2 wherein the N-bit CRC is a 16 bit CRC.

4. (ORIGINAL) The method as defined in claim 3 wherein K=2 and J=8.

5. (ORIGINAL) The method as defined in claim 1 wherein the generator polynomial is $x^{16}+x^{12}+x^5+1$.

Claims 6-13 (CANCELLED).